Claims

[c1] What is claimed is:

1. A method for performing a delay lock to generate a second clock according to a first clock and to synchronize the second clock with the first clock, the method comprising:

executing a plurality of correcting processes, each of which increases or decreases by a respective correction interval a respective delay time between corresponding periods of the first clock and the second clock;

wherein a subsequent correction interval for a subsequent correcting process is substantially half a previous correction interval of a previous correcting process.

[c2] 2. The method of claim 1, wherein the correcting process further comprises:

determining if the first clock and the second clock are synchronized and generating a corresponding comparison result;

wherein the delay time between the corresponding periods of the first clock and the second clock for the subsequent correcting process is increased or decreased by the subsequent correction interval according to the comparison result.

[c3] 3. The method of claim 2, wherein determining if the corresponding periods of the first clock and the second clock are synchronized is decided by comparing the time interval between a period of the second clock and a corresponding reference period of the first clock.

[c4] 4. The method of claim 1 further comprising:

prior to the plurality of correcting processes, setting the correction interval to a predetermined initial value..

[c5] 5. The method of claim 1, wherein the method is used for a delay lock circuit, the delay lock circuit comprising:

a delayer for delaying the second clock in order to change the delay time between the corresponding periods of the second clock and the first clock;

wherein when the delay time between the corresponding periods of the first clock and the second clock is increased or decreased by the correction interval, the delayer is used to delay the second clock so that the delay time between the corresponding periods of the first clock and the second clock is modified.

[c6] 6. The method of claim 5, wherein the delayer comprises a plurality of delay units, each of the delay units capable of increasing the delay time between the corresponding periods of the first clock and the second clock by a unit delay time.

[c7] 7. The method of claim 5, wherein the delay lock circuit further comprises a comparator electrically connected to the delayer for determining if the corresponding periods of the first clock and the second clock are synchronized and generating a corresponding comparison result; wherein the delay time between the corresponding periods of the first clock and the second clock is increased or decreased by the correction interval according to the comparison result.

[c8] 8. The method of claim 7, wherein the comparator compares the time interval between a period of the first clock and a corresponding reference period of the second clock to generate the comparison result; wherein the period of the first clock corresponding to the period of the second period leads the reference period by a predetermined reference interval.

[c9] 9. The method of claim 5, wherein the delay lock circuit further comprises a register to store information about the correction interval.

[c10] 10. The method of claim 1 further comprising:
terminating the plurality of correcting processes when the correction interval is smaller than a predetermined value.

[c11]

11. A delay lock circuit for generating a second clock according to a first clock and synchronizing the first clock and the second clock, the delay lock circuit comprising:
a comparator for determining if corresponding periods of the first clock and the second clock are synchronized and generating a corresponding comparison signal;
a delayer electrically connected to the comparator for delaying the second clock so as to change a delay time between the corresponding periods of the first clock and the second clock; and
a controller to control the delay lock circuit;
wherein the controller uses the delayer to perform a correcting process to increase or decrease the delay time between the corresponding periods of the first clock and the second clock by a correction interval, wherein a subsequent correction interval of a

subsequent correcting process is substantially half of aprevious correction interval of a previous correcting process.

[c12] 12. The delay lock circuit of claim 11, wherein the delayer comprises a plurality of delay units, each of the delay units capable of increasing the delay time between the corresponding periods of the first clock and the second clock by a unit delay time.

[c13] 13. The delay lock circuit of claim 11, wherein the delay lock circuit further comprises a register to store information about the correction interval.

[c14] 14. The delay lock circuit of claim 11, wherein the comparator compares the time interval between a period of the second clock and a corresponding reference period of the first clock to generate the comparison signal, wherein the period of the first clock corresponding to the period of the second clock leads the reference clock by a predetermined reference interval.

[c15] 15. The delay lock circuit of claim 11, wherein if the correction interval is smaller than a predetermined value, the controller terminates the correcting process.